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(54) "IMPROVEMENTS IN OR RELATING TO DATA PROCESSING SYSTEMS"

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company, of Berlin and Munich, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to data processing systems.

The processing of logic and arithmetic commands of programmes is carried out in the calculating unit of the central part of a data processing system. The calculating unit must be capable of executing various operations. If the processing requires that operands be linked several times, then it is necessary to provide several cycles through the logic unit. This, of course, increases processing time.

In modern data processing units, processing must be as rapid as possible. In addition it should also be possible to carry out monitoring of the calculating unit, with respect to transmission and processing faults, during normal command processing.

The aim exists to provide a data processing system, in which the processing can be effected particularly rapidly and in which it is possible to monitor the operand processing.

According to the present invention there is provided a data processing system comprising a central unit containing only one calculating unit, the calculating unit including a plurality of logic units, wherein each of said logic units is adapted to process full data width operands, and wherein said logic units are operable in a first state in which they execute respective operations on respective operands independently of one another and in a second state in which they execute like operations.

"Full data width" corresponds to the data width of the multi-purpose registers and of the data busbar in the central unit. The logic units contain not only adders, but also registers and shift registers.

The logic units are advantageously constructed in such manner that they may be connected to one another. In this case preferably when in said second state the logic units are interconnected in such manner that they act in the manner of a single logic unit so that an operand having a width greater than the full data width may be processed in one cycle. This is particularly advantageous in processing in floating point arithmetic.

In said first state the logic units operate independently of one another, so that each logic unit can be supplied with various operands, these operands can be linked in various manners in the logic units and the results can be separately analysed. This simultaneous operation results in a considerable reduction in the length of the processing time. If there are two logic units in the calculating unit, the processing time is halved.

It is also possible to detect faults which have arisen in the transmission and linking of operands. To this end the same operands are conducted to the logic units when in said first state and are linked in identical fashion. The results from the various logic units are checked for identity with the aid of a comparator. In the event of identity the command proceeds in normal fashion. In the case of non-identity, a signal indicating a fault is produced to interrupt command execution, save the command address, and instigate a fault diagnosis routine. Naturally the same checking process can also take place in the processing of simple address calculations. This monitoring does not involve a lengthening of the command duration.

It is also possible to check the logic units or parts thereof even when no operands are being linked. Thus if for example no logic unit is required in the course of the command processing, the logic units are loaded with arbitrary operands in identical fashion and are set for identical operations. The logic units operate independently of one another. Advantageously the logic units are arranged to execute those operations which cannot be checked in the normal sequence. Here again, the logic results are compared with one another, and in the event of non-identity, a fault signal is emitted. If a fault signal occurs, the command processing is interrupted as described above. If no fault signal occurs, the command processing is not

impaired in any way.

If a shift device is provided in the logic unit, its function too may be checked. The same operands are introduced into the shift devices in the various logic units, shift commands are executed, and then the result is compared during the transfer process.

The present invention will now be described by way of example and with reference to the drawings, in which:--

Figure 1 is a block circuit diagram of a data processing system in accordance with the present invention; and

Figure 2 is a more detailed diagram of the calculating unit forming part of the system shown in Figure 1.

The data processing system shown in the drawing comprises a working store ASP which is directly connected to a calculating unit RW, in fact to two operand registers B1 and B2 contained therein. The calculating unit is also connected to a register set RES. The register set RES contains multi-purpose registers which may be approached by the programmer. Each multi-purpose register is provided in duplicate (block A and block B). Both blocks always possess the same contents, but can be read out separately. This enables command acceleration in the case of register – register-commands.

The calculating unit comprises two logic units VE1 and VE2. The inputs of each logic unit are connected to two operand storage registers A1, B1 and A2, B2, each pair serving to accommodate one pair of operands, which are to be linked in the associated logic unit. The registers A1, B1 and A2, B2 can be shift registers. Each logic unit VE1, VE2 consequently deals with one pair of operands. The pair of operands can either be input into the operand storage registers in parallel fashion in which case the registers A1 and A2, and B1 and B2 respectively contain the same information (identical pairs of operands), or they can be input consecutively, in which case the registers A1, A2, B1 and B2 can contain different information (= different pairs of operands). Each logic unit can optionally supply its output information either to the working store ASP, to the register set RES, or to its associated pair of operand storage registers A1, B1 or A2, B2. Intermediate storage registers ZSP1 and ZSP2 serve to intermediately store the output information from the logic units in the case of supply to the register set RES or the working store ASP. The outputs of the logic units are connected to one another via a compatator VG.

The various units shown can be designed in known fashion. Thus the logic units VE contain adders and register sets, the comparator circuit VG can consist of an EXCLUSIVE–OR element, the intermediate storage registers ZSP contain register sets and the working store ASP can be a core store or semiconductor store.

If two different pairs of operands are to be processed simultaneously in the calculating unit RW, one pair of operands is conducted to the operand register pair A1, B1 and the other pair of operands is conducted to the operand register pair A2, B2. From there, the one pair of operands passes into the one logic unit VE1, and the other pair of operands passes into the other logic unit VE2. The operands are linked in these logic units VE1 and VE2 in accordance with the commands to be processed. The information resulting from this linking is intermediately stored in the intermediate storage registers ZSP1 and ZSP2, or in the pairs of operand registers A1, B1 and A2, B2 respectively, and is then conducted back into the working store ASP or is conducted to the register set RES.

If it is intended to carry out a check of the transmission or the processing of operands, the pairs of operands are loaded in parallel fashion into the pairs of operand registers A1, B1 and A2, B2. The logic units VE1 and VE2 are set to the same operation. The same pair of operands is then linked in identical fashion both in the logic unit VE1 and in the logic unit VE2. If the logic units are operating correctly and no faults have arisen in the transmission of the operands, the logic results at the output of the logic unit VE1 and at the output of the logic unit VE2 must be identical. This is checked with the aid of the comparator VG. In the case of identity, the one logic result can for example be stored back into the working store ASP. The other logic result is superfluous. If, however, the comparator VG indicates non-identity, it emits a signal which characterises the existence of a fault. Then the location of the fault within the central unit can be established for example with the aid of a test programme.

To process operands which have a large data width, for example are twice as long as full data width operands, the logic units VE1 and VE2 can, in the present system, be interconnected and set at identical operations. Then the logic units will act as one single logic unit.

The Figure shows only the data channels, the lines for the control signals have been omitted.

Thus with the above system it is possible to achieve with a low outlay approximately substantially the same effect as in reliable calculating systems which consist for example of two parallel operating computers. Through the use of a plurality of logic units it is possible to accelerate the speed of the command processing of a programme. Finally double width operands can be dealt with in one single cycle. Furthermore, it is also possible to check out the calculating unit during normal operations, as well as during periods when the latter is not used for the processing.

WHAT WE CLAIM IS:–

1. A data processing system comprising a central unit containing only one calculating

unit, the calculating unit including a plurality of logic units, wherein each of said logic units is adapted to process full data width operands, and wherein said logic units are operable in a first state in which they execute respective operations on respective operands independently of one another and in a second state in which they execute like operations.

2. A system as claimed in Claim 1 wherein when in said second state the logic units are interconnected in such manner that they act in the manner of a single logic unit so that an operand having a width greater than the full data width may be processed in one cycle.

3. A system as claimed in Claim 1 or 2, wherein when in said first state the logic units are for checking purposes arranged to execute the same operations on the same operands, and wherein a comparator is provided and is arranged to compare the logic results of said operations with one another and to provide a signal indicating a fault in the event of non-identity.

4. A data processing system substantially as herein described with reference to the accompanying drawings.

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1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

Fig. 1

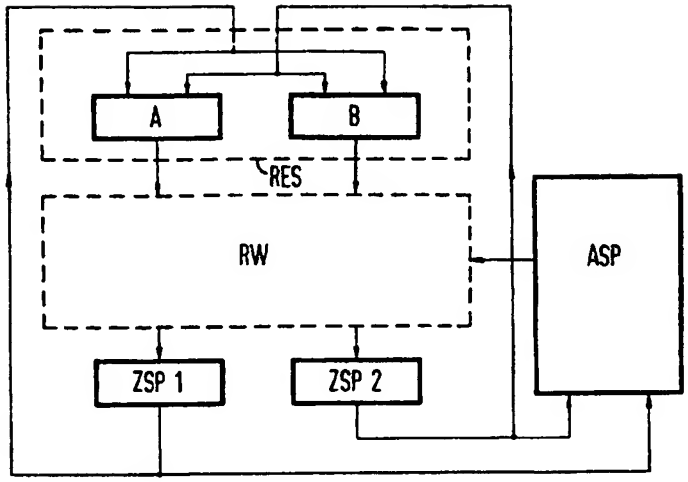

Fig. 2